a testing circuit configured to output a test signal, which is supplied from the exterior during a testing mode, as said second adjusting signal and to output the logic values stored in said programming circuit to said power on resetting circuit and said voltage generator, respectively, as said first adjusting signal and said second adjusting signal during a normal operation mode.

8. (New) The semiconductor integrated circuit according to claim 7, wherein said testing circuit includes a mask circuit for masking an output from said programming circuit and for outputting a testing signal as said second adjusting signal, in response to a test activating signal which is activated during said testing mode.

9. (New) The semiconductor integrated circuit according to claim 7, wherein said programming circuit includes fuses configured to program the logical values of said first adjusting signal and said second adjusting signal. --

REMARKS

Claims 1-9 are pending. By this Amendment the title has been amended and claims 1-3 have merely been amended to particularly point out and distinctly claim the invention. Therefore, it is submitted that these amendments do not narrow the scope of any element of any claim. Claims 7-9 are newly added. No new matter is presented. Accordingly, claims 1-9 are presented for consideration.

Claims 2-6 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Specifically, with respect to claim 2, the Office Action took the position that the limitation "timing changing circuit changes said inactivation circuit corresponding to a threshold voltage of transistors implemented in said internal circuit" is misdescriptive

because the inactivation is adjusted by fuse circuit 18 as disclosed in Fig. 2 and page 7 of the Specification. The Office Action further took the position that, with respect to claim 3, the limitation "timing changing circuit changes said inactivation timing corresponding to said internal supply voltage which varies with a threshold voltage of transistors implemented in said voltage generator" also appears to be misdescriptive.[1] By this amendment claims 2 and 3 have been amended, thereby rendering the rejection moot. Therefore, Applicants respectfully request that the rejection be withdrawn.

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Lee (U.S. Patent No. 6,040,722). Applicants respectfully submit that claim 1 recites subject matter that is neither disclosed nor suggested in Lee.

Claim 1 recites a semiconductor integrated circuit including a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit and for inactivating the reset signal for a predetermined period after the initial supply to terminate an initialization of the internal circuit. A timing changing circuit is provided for adjusting the predetermined period.

Claim 7 recites a semiconductor integrated circuit including a power-on resetting circuit having a transistor. The power-on resetting circuit is configured to inactivate a reset signal which initializes an internal circuit after activating the reset signal for a predetermined period, in response to a power supply being switched on, by utilizing a threshold voltage of the transistor. The power-on resetting circuit changes the time that the reset signal is inactivated in accordance to a first adjusting signal. A voltage

[1] The Office Action has inadvertently referred to this limitation as being recited in claim 2.

generator includes a transistor and is configured to generate an internal supply voltage in accordance with an external supply voltage by utilizing a threshold voltage of the transistor. The voltage generator varies the level of the internal supply voltage in accordance to a second adjusting signal. A timing changing circuit includes a programming circuit configured to store logic values of the first adjusting signal and the second adjusting signal and a testing circuit. The testing circuit is configured to output a test signal that is supplied from the exterior during a testing mode as the second adjusting signal, and to output the logic values stored in the programming circuit to the power-on resetting circuit and the voltage generator, respectively, as the first adjusting signal and the second adjusting signal during a normal operation mode.

The Office Action took the position that Lee discloses the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest such structure and, therefore, fails to provide the advantages that are provided by the present invention. For example, the present invention adjusts the time that the reset signal is inactivated by using the timing changing circuit. This prevents the reset signal from inactivating before the initialization of the internal circuit terminates and allows reliable initialization of the internal circuit, as discussed in Applicant's Specification at page 3. Additionally, the present invention enables adjustment of the time that the reset signal is inactivated without directly measuring the timing of the reset signal by utilizing the voltage generator transistor, as recited in claim 7, and as discussed in Applicant's Specification at page 15. No such configuration is disclosed in Lee.

Lee discloses a power-on reset circuit for generating a power-on reset signal when a power supply potential is applied. The power-on reset circuit is integrated in a device chip together with an internal circuits that has sequential logics or memory devices. The power-on reset signal is applied after an adjustable time interval to reset to desired logic states.. However, Lee only discloses adjusting the timing that the resetting of the sequential logic circuits or the memory device initiates by controlling the timing that the power-on reset signal activates. This is contrary to the present invention which adjusts the timing that the reset signal inactivates by using the timing changing circuit, as recited in claim 1, so that the timing that the initialization of the internal circuit terminates is made to be appropriate.

Additionally, Lee does not disclose a voltage generator that operates in response to a second adjusting signal that the timing changing circuit outputs, nor a testing circuit that outputs a testing signal from the exterior as a second adjusting signal during the testing mode, as recited by claim 7. Upon review on consideration of Lee, it appears that Lee only discloses a counter that stores the value of the signal that adjusts the timing the reset is inactivated.

As claims 2-6 depend from independent claim 1, and claims 8 and 9 depend from independent claim 7, Applicants submit that these claim also recite subject matter that is neither disclosed nor suggested by the prior art, for at least the reasons set forth above.

Furthermore, the Office Action asserted that the merit of claims 2-6 could not be determined due to the "severity of indefiniteness" noted. However, Applicant respectfully submits that the claims as submitted are clear and that each of claims 2-6

recite subject matter that particularly points out and distinctly claims the invention. Therefore, in the event claims 2-6 are not found to be allowable, Applicant requests that a non-final Office Action be issued addressing the subject matter of these claims.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1-9, and the prompt issuance of a Notice of Allowability are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108397-00042**.

Respectfully submitted,
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Enclosure: Marked-up Version of Claims
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Marked-Up Version of Claims

1. (Amended) A semiconductor integrated circuit comprising:

a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize [which initializes] an internal circuit, [for a predetermined period after a power supply is switched on,] and [then] for inactivating the reset signal for a predetermined period after the initial supply to terminate an initialization of the internal circuit; and

a timing changing circuit for [changing an inactivation timing of said reset signal] adjusting the predetermined period.

2. (Amended) The semiconductor integrated circuit according to claim 1, wherein said timing changing circuit changes [said] an inactivation timing of the reset signal in accordance with a first set of signals [corresponding to a threshold voltage of transistors implemented in said internal circuit].

3. (Amended) The semiconductor integrated circuit according to claim 1, further comprising a voltage generator for generating an internal supply voltage in accordance with an external supply voltage, and wherein

said timing changing circuit changes [said] an inactivation timing of the reset signal corresponding to said internal supply voltage [which varies with a threshold voltage of transistors implemented in said voltage generator].